



DPW

Docket No.: M4065.0100/P100-B
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Howard E. Rhodes

Application No.: 10/617,706

Filed: July 14, 2003

For: CMOS IMAGER WITH SELECTIVELY
SILICIDED GATES

Confirmation No.: 3719

Art Unit: 2814

Examiner: N. V. Ngo

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the restriction requirement set forth in the Office Action mailed July 1, 2004 (Paper No. Mail Date 0604), Applicant hereby elects Group I claims 87-128 for continued examination without traverse.

The Examiner has required restriction between the following:

Group I – Claims 87-128, drawn to a semiconductor device; and

Group II – Claims 17-70, drawn to a process for making a semiconductor device.

Dated: July 7, 2004

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

Elizabeth Parsons

Registration No.: 52,499

DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorneys for Applicant